Amendments to the Claims:

The listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A system for transferring a signal to a channel, comprising:

a storage unit associated with the channel for storing source identification information of a plurality of sources and indicating an order of priority of the plurality of sources for access to the channel;

a plurality of selection circuits for receiving input signals from the sources, each of the selection circuits selecting one of the plurality of input signals; and

a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel, such that the signal is forwarded to the channel according to the priorities associated with the sources.

2. (Original) The system of claim 1, wherein each selection circuit selects the selected input signal according to a state of a respective control input to the selection circuit.

3. (Original) The system of claim 1, wherein the storage unit is a register.

4. (Original) The system of claim 1, wherein the storage unit stores the source identification information for the sources in order of priority of the sources for access to the channel.

5. (Original) The system of claim 1, wherein the storage unit stores the source identification information for a highest-priority source in the most significant bits of the storage unit.

6. (Original) The system of claim 1, wherein the storage unit sequentially stores the source identification information according to priority from the most significant bits to

the least significant bits of the storage unit.

7. (Original) The system of claim 1, wherein the storage unit sequentially stores the source identification information according to priority from the least significant bits to the most significant bits of the storage unit.

8. (Original) The system of claim 1, wherein the circuit checks the outputs of the selection circuits in a predetermined sequence.

9. (Original) The system of claim 8, wherein the circuit sequentially checks the outputs of the selection circuits.

10. (Original) The system of claim 8, wherein the sequence is determined by an order in which the source identification information of the sources is stored in the storage unit.

11. (Original) The system of claim 1, wherein the circuit checks the outputs of the selection circuits in order of priority of the sources for forwarding input signals to the channel.

12. (Original) The system of claim 1, wherein the system includes a plurality of channels, input signals from the sources being able to be forwarded to the plurality of channels.

13. (Original) The system of claim 12, further comprising a plurality of storage units associated respectively with the plurality of channels.

14. (Original) The system of claim 13, wherein each of the storage units stores source identification information for sources that are able to forward input signals onto the channel associated with the storage unit.

15. (Original) The system of claim 1, wherein the selection circuits are multiplexers.

16. (Original) The system of claim 15, wherein the multiplexers are ordered according to the sequence of the source identification information stored in the storage unit.

17. (Original) The system of claim 16, wherein the multiplexers are ordered according to priorities of the sources for forwarding input signals to the channel.

18. (Original) The system of claim 1, wherein the sources are applied to inputs of the selection circuits according to a predetermined order.

19. (Original) The system of claim 18, wherein the predetermined order depends on priority of the sources for access to the channel.

20. (Original) The system of claim 18, wherein the source identification information is generated according to the predetermined order such that the selection circuits select the sources based on priority of the sources for access to the channel.

21. (Original) The system of claim 1, further comprising a channel unit associated with the channel for processing information related to the channel.

22. (Original) The system of claim 21, wherein the storage unit is part of the channel unit.

23. (Currently Amended) A system for transferring [[a]]signals to channels, comprising;

a plurality of storage units, each storage unit being associated with one of the channels, and each storage unit being adapted to store source identification information for each of the sources that can transfer input signals to the associated channel and indicating an order of priority of the sources for access to the channel;

for each of the plurality of channels, a plurality of selection circuits for receiving input signals from the sources, each of the selection circuits selecting one of the plurality of input signals; and

for each of the plurality of channels, a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel, such that the signals are forwarded to the channels according to the priorities associated with the sources.

24. (Original) The system of claim 23, wherein each selection circuit selects the selected input signal according to a state of a respective control input to the selection circuit.

25. (Original) The system of claim 23, wherein one or more of the sources are allocated to one or more of the channels.

26. (Original) The system of claim 25, wherein the allocation of the sources to the channels is controllable by controlling storage of source identification information in the storage units.

27. (Original) The system of claim 23, wherein the storage units are registers.

28. (Original) The system of claim 23, wherein each of the storage units stores its source identification information for the sources in order of priority of the sources for access to the associated channel.

29. (Original) The system of claim 23, wherein the selection circuits are multiplexers.

30. (Original) The system of claim 29, wherein the multiplexers are ordered according to the sequence of the source identification information stored in the storage unit.

31. (Original) The system of claim 29, wherein the multiplexers are ordered according to priorities of the sources for forwarding input signals to the channels.

32. (Original) The system of claim 23, wherein the sources are applied to inputs of

the selection circuits according to a predetermined order.

33. (Original) The system of claim 32, wherein the predetermined order depends on priority of the sources for access to the channels.

34. (Original) The system of claim 32, wherein the source identification information is generated according to the predetermined order such that the selection circuits select the sources based on priority of the sources for access to the channels.

35. (Original) The system of claim 23, further comprising a plurality of channel units associated respectively with the plurality of channels for processing information related to the channels.

36. (Original) The system of claim 35, wherein each of the storage units is part of one of the channel units.

37. (Currently Amended) A direct memory access (DMA) controller for controlling transfer of signals from input sources to output devices, a plurality of channels being connected to the output devices, the DMA controller comprising:

a plurality of storage units, each storage unit being associated with one of the channels, and each storage unit being adapted to store source identification information for each of the sources that can transfer input signals to the associated channel and indicating an order of priority of the sources for access to the channel;

for each of the plurality of channels, a plurality of selection circuits for receiving input signals from the sources, each of the selection circuits selecting one of the plurality of input; and

for each of the plurality of channels, a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel, such that the signals are forwarded to the channel according to the priorities associated with the sources.

38. (Original) The DMA controller of claim 37, wherein each selection circuit selects the selected input signal according to a state of a respective control input to the selection

circuit.

39. (Original) The DMA controller of claim 37, wherein one or more of the sources are allocated to one or more of the channels.

40. (Original) The DMA controller of claim 37, wherein the allocation of the sources to the channels is controllable by controlling storage of source identification information in the storage units.

41. (Original) The DMA controller of claim 37, wherein the storage units are registers.

42. (Original) The DMA controller of claim 37, wherein each of the storage units stores its source identification information for the sources in order of priority of the sources for access to the associated channel.

43. (Original) The DMA controller of claim 37, wherein the selection circuits are multiplexers.

44. (Original) The DMA controller of claim 43, wherein the multiplexers are ordered according to the sequence of the source identification information stored in the storage unit.

45. (Original) The DMA controller of claim 43, wherein the multiplexers are ordered according to priorities of the sources for forwarding input signals to the channels.

46. (Original) The DMA controller of claim 37, wherein the sources are applied to inputs of the selection circuits according to a predetermined order.

47. (Original) The DMA controller of claim 46, wherein the predetermined order depends on priority of the sources for access to the channels.

48. (Original) The DMA controller of claim 46, wherein the source identification information is generated according to the predetermined order such that the selection circuits select the sources based on priority of the sources for access to the channels.

49. (Original) The DMA controller of claim 37, further comprising a plurality of channel units associated respectively with the plurality of channels for processing information related to the channels.

50. (Original) The DMA controller of claim 40, wherein each of the storage units is part of one of the channel units.

51. (Currently Amended) A method for transferring a signal to a channel, comprising:

storing source identification information for a plurality of sources and indicating an order of priority of the plurality of sources for access to the channel in a storage unit associated with the channel;

providing a plurality of selection circuits for receiving input signals from the sources, each of the selection circuits selecting one of the plurality of input signals;

with a checking circuit, checking outputs of the selection circuits and forwarding a selected input signal to the channel, such that the signal is forwarded to the channel according to the priorities associated with the sources.

52. (Original) The method of claim 51, wherein each selection circuit selects the selected input signal according to a state of a respective control input to the selection circuit.

53. (Original) The method of claim 51, wherein the storage unit is a register.

54. (Original) The method of claim 51, wherein the storage unit stores the source identification information for the sources in order of priority of the sources for access to the channel.

55. (Original) The method of claim 51, wherein the storage unit stores the source identification information for a highest-priority source in the most significant bits of the storage unit.

56. (Original) The method of claim 51, wherein the storage unit sequentially stores the source identification information according to priority from the most significant bits to the least significant bits of the storage unit.

57. (Original) The method of claim 51, wherein the storage unit sequentially stores the source identification information according to priority from the least significant bits to the most significant bits of the storage unit.

58. (Original) The method of claim 51, wherein the circuit checks the outputs of the selection circuits in a predetermined sequence.

59. (Original) The method of claim 58, wherein the circuit sequentially checks the outputs of the selection circuits.

60. (Original) The method of claim 58, wherein the sequence is determined by an order in which the source identification information of the sources is stored in the storage unit.

61. (Original) The method of claim 51, wherein the checking circuit checks the outputs of the selection circuits in order of priority of the sources for forwarding input signals to the channel.

62. (Original) The method of claim 51, wherein the communication system includes a plurality of channels, input signals from the sources being able to be forwarded to the plurality of channels.

63. (Original) The method of claim 62, further comprising providing a plurality of

storage units associated respectively with the plurality of channels.

64. (Original) The method of claim 63, wherein each of the storage units stores source identification information for sources that are able to forward input signals onto the channel associated with the storage unit.

65. (Original) The method of claim 51, wherein the selection circuits are multiplexers.

66. (Original) The method of claim 65, wherein the multiplexers are ordered according to the sequence of the source identification information stored n the storage unit.

67. (Original) The method of claim 65, wherein the multiplexers are ordered according to priorities of the sources for forwarding input signals to the channel.

68. (Original) The method of claim 51, wherein the sources are applied to inputs of the selection circuits according to a predetermined order.

69. (Original) The method of claim 68, wherein the predetermined order depends on priority of the sources for access to the channel.

70. (Original) The method of claim 68, wherein the source identification information is generated according to the predetermined order such that the selection circuits select the sources based on priority of the sources for access to the channel.

71. (Original) The method of claim 51, further comprising a channel unit associated with the channel for processing information related to the channel.

72. (Original) The method of claim 71, wherein the storage unit is part of the channel unit.